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	Mail Stop Appeal Brief-Patents **Commissioner for Patents** **P. O. Box 1450** **Alexandria, VA 22313-1450**		
From:	**Rachel V. Leiterman**		
Serial No.:	**09/846,980**		
Docket:	**M-9635 US (LUM-M-9635 US)**		
Re:	**Reply Brief Under 37 CFR §1.193**		
Pages:	**35 (including cover sheet)**		

Message:

Re: Applicant(s): Stephen A. Stockman; Serge L. Rudaz; Mira S. Misra
Assignee: Lumileds Lighting U.S., LLC
Title: Forming Low Resistivity P-Type Gallium Nitride
Serial No.: 09/846,980
Examiner: Matthew J. Song Filed: April 30, 2001
Docket No.: M-9635 US Group Art Unit: 1765

Dear Sir:

Transmitted herewith are the following documents in the above-identified application:

(1) Transmittal Letter (1 page);
(2) Reply Brief (11 pages in triplicate).

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Re:	Applicant(s):	Stephen A. Stockman; Serge L. Rudaz; Mira S. Misra	
	Assignee:	Lumileds Lighting U.S., LLC	
	Title:	Forming Low Resistivity P-Type Gallium Nitride	
	Serial No.:	09/846,980	
	Examiner:	Matthew J. Song	Filed: April 30, 2001
	Docket No.:	M-9635 US	Group Art Unit: 1765

Dear Sir:

Transmitted herewith are the following documents in the above-identified application:

(1) This Transmittal Letter (1 page);
(2) Reply Brief Under 37 CFR §1.193 (11 pages in triplicate).

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Rachel V. Leiterman
Attorney for Applicant(s)
Reg. No. 46,868

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Applicants:	Stephen A. Stockman; Serge L. Rudaz; Mira S. Misra		
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August 23, 2004

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REPLY BRIEF UNDER 37 CFR § 1.193

Dear Sir:

Applicants submit this Reply Brief pursuant to 37 C.F.R. 1.193(b), in response to the Examiner's Answer mailed June 21, 2004. The Commissioner is hereby authorized to deduct any amounts required for this reply brief and to credit any amounts overpaid to Deposit Account No. 502226.

The Examiner argues "Bour et al merely teaches a post-growth anneal is not required and preference towards not performing a post-growth anneal. Bour et al is solely concerned with acceptor activation, while Furukawa et al is also concerned with reducing lattice defects and lowering resistivity. Appellants have not considered the teachings of Furukawa et al, which provide motivation to one of ordinary skill at the time of the invention to improve the activation yield **and** reduce lattice defects, resulting in a superior product compared to a p-type GaN layer, which is not annealed according to the process taught by Furukawa et al." See page 7 of the Examiner's Answer, emphasis in original.

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Applicants respectfully submit that the teachings of Bour et al. and Furukawa et al. do not provide a motivation to tolerate the problems described by Bour et al. caused by an anneal as taught by Furukawa et al. Bour et al. implies that an in-situ acceptor activation as taught by Bour et al. results in the same level of acceptor activation as the type of anneal taught by Furukawa et al., without the problems caused the type of anneal taught by Furukawa et al. Accordingly, in order to combine Bour et al. and Furukawa et al., the motivation to combine must be independent from acceptor activation. The Examiner cites reduced lattice defects as this independent motivation. However, the language of Furukawa et al. indicates that the reduced lattice defects cited by the Examiner as a motivation to combine Furukawa et al. with Bour et al. would actually arise from **any** process that causes acceptor activation, including the process of Bour et al.

1. Bour et al. teaches a process resulting in the same level of acceptor activation as an anneal of the type taught by Furukawa et al.

Bour et al. teaches a process designed to **replace** the type of anneal taught by Furukawa et al. See, for example, column 1, lines 51-54, which state "it is an object of this invention to provide an in-situ thermal process for acceptor activation for Group III-V nitride compound semiconductors." The language of Bour et al. suggests that the same level of acceptor activation can be achieved using the technique of Bour et al. as using an anneal of the type taught by Furukawa et al. See, for example, column 6, lines 11-19, which describes Bour et al.'s first embodiment, an in-situ acceptor activation: "acceptor activation is the process of atomic H weakly bonded to Mg or Zn dopant atoms that are broken by a thermal anneal process over a sufficient period of time. The activation process should be easily carried out in a period of about 5 minutes to about 20 minutes depending, of course, on the reactor temperature. After the proper length of time to achieve activation, the reactor is permitted to

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cool down to room temperature so that substrate 17 may be removed from the reactor for further processing." The last two sentences of this passage in Bour et al. suggest that the process taught by Bour et al. can be adjusted, for example by adjusting temperature or time, to achieve the same acceptor activation result as the type of anneal taught by Furukawa et al. Nothing in Bour et al. teaches or suggests that the process advocated by Bour et al. results in inferior acceptor activation than the type of anneal taught by Furukawa et al. As a result, absent some other motivation unrelated to acceptor activation, there can be no motivation to tolerate the problems associated with Furukawa et al.'s anneal when Bour et al. teaches a method that avoids the anneal and results in the same level of acceptor activation.

2. Furukawa et al. teaches that reduction in defects arises from any acceptor activation process, including the process of Bour et al.

The Examiner cites reducing crystal defects as a motivation, unrelated to acceptor activation, to combine Bour et al. and Furukawa et al. However, Furukawa et al. clearly states that reduced crystal defects is a result of improved acceptor activation, and thus any process that improves acceptor activation, including the process of Bour et al., would be expected to result in reduced crystal defects. See, for example, the last sentence of the abstract, which states "[a]ccording to the annealing process, the p-type impurity can be more effectively activated, so that p-type gallium nitride compound semiconductor layers which have fewer crystal defects, etc. and have lower resistivity can be formed." The construction of this sentence indicates that "fewer crystal defects" is an effect of "the p-type impurity [is] more effectively activated." Though in the case of Furukawa et al., the desired activation is a result of Furukawa et al.'s annealing process, a person of skill in the art would expect that any process that effectively activates acceptors, including the process of Bour et al., would result in fewer crystal defects and lower resistivity. Accordingly, since Bour et al.'s process is

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expected to result in the same benefits as the anneal of Furukawa et al., there is no motivation to tolerate the problems associated with Furukawa et al.'s anneal by combining it with Bour et al.

In conclusion, as set forth in Applicants' Appeal Brief, Applicants believe that Bour et al. teaches away from combination with Furukawa et al., and therefore Bour et al. and Furukawa et al. cannot be combined. In addition, as set forth above, Applicants respectfully submit that given the teachings of Bour et al. and Furukawa et al., a person of skill in the art would expect that the process described by Bour et al. would result in the same acceptor activation and would provide the same benefit of reduced crystal defects as the anneal taught by Furukawa et al. As a result, there is no motivation to combine Bour et al. and Furukawa et al. and by doing so tolerate the problems of Furukawa et al.'s anneal described by Bour et al.

Applicants respectfully request that the Examiner's rejection be reversed.

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R Leiterman 8/23/04

Signature Date

Respectfully submitted,

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APPENDIX

1. A method for manufacturing a p-type III-V nitride compound semiconductor comprising:

growing in a chamber a III-V nitride compound semiconductor layer at a first temperature while introducing acceptor impurities into said layer to form an acceptor-doped layer, said chamber containing one or more gases providing hydrogen such that said hydrogen passivates at least some of said acceptor impurities;

cooling said acceptor-doped layer to a second temperature significantly lower than said first temperature during a cool-down process;

preventing additional hydrogen from diffusing into said acceptor-doped layer substantially during the cool-down process;

causing said acceptor-doped layer to be a p-type layer, having p-type conductivity and a hole density between approximately $3x10^{15}cm^{-3}$ and $1x10^{18}cm^{-3}$, after said cool-down process; and

after said cooling, heating said p-type layer to a third temperature greater than the second temperature and less than 625°C to remove hydrogen from said p-type layer thereby increasing said hole density and lowering the resistivity of said p-type layer.

3. The method of Claim 1 wherein said preventing additional hydrogen from diffusing into said acceptor-doped layer comprises preventing gases containing hydrogen from entering said chamber during said cool-down process and removing hydrogen in said chamber during said cool-down process.

4. The method of Claim 1 wherein said preventing additional hydrogen from diffusing into said acceptor-doped layer comprises forming an n-type semiconductor layer cap over said acceptor-doped layer prior to said cool-down process.

5. The method of Claim 1 wherein said causing said acceptor-doped layer to be a

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p-type layer prior to said annealing comprises treating a surface of said acceptor-doped layer to increase said hole density at said surface to be greater than $3x10^{15}cm^{-3}$.

6. The method of Claim 5 wherein said treating said surface comprises chemically etching said surface.

7. The method of Claim 5 wherein said treating said surface comprises plasma etching said surface.

8. The method of Claim 5 wherein said treating said surface comprises plasma cleaning said surface.

9. The method of Claim 5 wherein said treating said surface comprises chemically cleaning said surface.

10. The method of Claim 9 wherein said chemically cleaning said surface comprises cleaning said surface in a solution of at least one of KOH, NaOH, and NH_4OH.

11. The method of Claim 5 wherein said treating said surface comprises ultrasonically cleaning said surface.

12. The method of Claim 5 wherein said treating said surface comprises irradiating said surface with an electron-beam.

13. The method of Claim 5 wherein said treating said surface comprises exposing said surface to electromagnetic radiation.

14. The method of Claim 1 wherein said growing an acceptor-doped layer results in acceptor impurities in said acceptor-doped layer having greater than 90% passivation prior to said cool-down process.

15. The method of Claim 1 wherein, after said cool-down process, said hole density is greater than $3x10^{16}cm^{-3}$.

16. The method of Claim 1 wherein said introducing acceptor impurities comprises doping said semiconductor layer to have a density of acceptor impurities greater than

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$5x10^{18}cm^{-3}$.

17. The method of Claim 1 wherein said annealing is carried out at a temperature in the range of 100-625°C.

18. The method of Claim 1 wherein said anncaling is carried out at a temperature below 400°C.

19. The method of Claim 1 wherein said growing in a chamber an acceptor-doped layer is performed in a chamber different from a chamber in which said p-type layer is annealed.

20. The method of Claim 1 wherein said annealing is carried out after said cool-down process prior to any further processing of said p-type layer.

21. The method of Claim 1 wherein said growing in a chamber an acceptor-doped layer further comprises growing a III-V nitride compound n-doped semiconductor layer to form a light emitting diode.

22. The method of Claim 21 wherein said acceptor-doped layer is grown subsequent to said n-doped semiconductor layer.

23. The method of Claim 1 further comprising growing additional one or more III-V nitride compound acceptor-doped layers and causing said additional one or more acceptor-doped layers to be p-type prior to said annealing.

24. The method of Claim 1 wherein said annealing is carried out solely to remove said hydrogen from said p-type layer.

25. The method of Claim 1 wherein said annealing is carried out to remove said hydrogen from said p-type layer as well as to anneal or alloy a p-type ohmic contact.

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26. The method of Claim 1 wherein said growing said acceptor-doped layer comprises growing a group III-V compound semiconductor including gallium and nitrogen.

27. The method of Claim 1 wherein said acceptor impurities comprise magnesium.

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28. The method of Claim 1 wherein said annealing is carried out in a gas environment containing N_2.

29. The method of Claim 1 wherein the resistivity of said p-type layer prior to said annealing is less than 5000 ohm-cm.

30. The method of Claim 1 wherein the resistivity of said p-type layer prior to said annealing is less than 30 ohm-cm.

31. A method for manufacturing a p-type III-V nitride compound semiconductor comprising:

growing in a chamber a III-V nitride compound semiconductor layer at a first temperature while introducing acceptor impurities into said layer to form an acceptor-doped layer, said chamber containing one or more gases providing hydrogen such that said hydrogen passivates at least some of said acceptor impurities;

cooling said acceptor-doped layer to a second temperature significantly lower than said first temperature during a cool-down process, thereby causing said acceptor-doped layer to be a p-type layer, having p-type conductivity and a hole density between approximately $3x10^{15}cm^{-3}$ and $1x10^{18}cm^{-3}$, after said cool-down process; and

after said cooling, heating said p-type layer to a third temperature greater than the second temperature and less than 625°C to remove hydrogen from said p-type layer thereby increasing said hole density and lowering the resistivity of said p-type layer.

32. The method of Claim 31 further comprising substantially preventing additional hydrogen from diffusing into said acceptor-doped layer during said cooling process.

33. The method of Claim 32 wherein said preventing additional hydrogen from diffusing into said acceptor-doped layer comprises preventing gases containing hydrogen from entering said chamber during said cool-down process and removing hydrogen in said chamber during said cool-down process.

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34. The method of Claim 32 wherein said preventing additional hydrogen from diffusing into said acceptor-doped layer comprises forming an n-type semiconductor layer cap over said acceptor-doped layer prior to said cool-down process.

35. The method of Claim 31 further comprising treating a surface of said acceptor-doped layer to increase said hole density at said surface to be greater than $3x10^{15}cm^{-3}$.

36. The method of Claim 35 wherein said treating said surface comprises chemically etching said surface.

37. The method of Claim 35 wherein said treating said surface comprises plasma etching said surface.

38. The method of Claim 35 wherein said treating said surface comprises plasma cleaning said surface.

39. The method of Claim 35 wherein said treating said surface comprises chemically cleaning said surface.

40. The method of Claim 39 wherein said chemically cleaning said surface comprises cleaning said surface in a solution of at least one of KOH, NaOH, and NH_4OH.

41. The method of Claim 35 wherein said treating said surface comprises ultrasonically cleaning said surface.

42. The method of Claim 35 wherein said treating said surface comprises irradiating said surface with an electron-beam.

43. The method of Claim 35 wherein said treating said surface comprises exposing said surface to electromagnetic radiation.

44. The method of Claim 31 wherein said growing an acceptor-doped layer results in acceptor impurities in said acceptor-doped layer having greater than 90% passivation prior to said cool-down process.

45. The method of Claim 31 wherein, after said cool-down process, said hole

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density is greater than $3x10^{16}cm^{-3}$.

46. The method of Claim 31 wherein said introducing acceptor impurities comprises doping said semiconductor layer to have a density of acceptor impurities greater than $5x10^{18}cm^{-3}$.

47. The method of Claim 31 wherein said annealing is carried out at a temperature in the range of 100-625°C.

48. The method of Claim 31 wherein said annealing is carried out at a temperature below 400°C.

49. The method of Claim 31 wherein said growing in a chamber an acceptor-doped layer is performed in a chamber different from a chamber in which said p-type layer is annealed.

50. The method of Claim 31 wherein said annealing is carried out after said cool-down process prior to any further processing of said p-type layer.

51. The method of Claim 31 wherein said growing in a chamber an acceptor-doped layer further comprises growing a III-V nitride compound n-doped semiconductor layer to form a light emitting diode.

52. The method of Claim 51 wherein said acceptor-doped layer is grown subsequent to said n-doped semiconductor layer.

53. The method of Claim 31 further comprising growing additional one or more III-V nitride compound acceptor-doped layers and causing said additional one or more acceptor-doped layers to be p-type prior to said annealing.

54. The method of Claim 31 wherein said annealing is carried out solely to remove said hydrogen from said p-type layer.

55. The method of Claim 31 wherein said annealing is carried out to remove said hydrogen from said p-type layer as well as to anneal or alloy a p-type ohmic contact.

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56. The method of Claim 31 wherein said growing said acceptor-doped layer comprises growing a group III-V compound semiconductor including gallium and nitrogen.

57. The method of Claim 31 wherein said acceptor impurities comprise magnesium.

58. The method of Claim 31 wherein said anncaling is carried out in a gas environment containing N_2.

59. The method of Claim 31 wherein the resistivity of said p-type layer prior to said anncaling is less than 5000 ohm-cm.

60. The method of Claim 31 wherein the resistivity of said p-type layer prior to said annealing is less than 30 ohm-cm.

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